THREE-LEVEL LEADFRAME FOR NO-LEAD PACKAGES

FIELD OF THE INVENTION

The present invention is related in general to the field of semiconductor devices and processes, and more specifically to the structure and material of leadframes for integrated circuit devices.

DESCRIPTION OF THE RELATED ART

When the flip-chip technology is used in the assembly of semiconductor devices, in spite of its frequently higher cost compared to wire bonding, it is often required in order to meet demanding performance goals. Among these performance goals are higher numbers of input/output (I/O) terminals, shorter electrical paths for higher speed and frequency, and lower heat dissipation paths for improved thermal performance. These performance goals are driven, for instance, by the pervasive growth of semiconductor products for the wireless and computer peripheral markets. Devices with a need for high frequency performance yet low I/O count include power amplifiers and optical transceivers.

In another trend in the semiconductor industry, driven by miniaturization of chips and packages, there is increased interest in small outline no-lead, or leadless, package types because of their chip-scale dimensions and lower material content and cost. These packages do not have leads, per se, but only land areas that are exposed on the bottom side of the package. Pressure contact or solder

joints are made to these land areas. Most often, however, no-lead packages are based on wire bonding technology. Only recently have no-lead packages been proposed in the literature for flip-chip assembly; these packages are, however, only suitable for low I/O count (8 to 100 I/O's).

In order to provide a no-lead package for a flip-chip assembled device of intermediate I/O count, a solution has to be found how to structure a leadframe from an original sheet of metal in order to produce an array of contact pads, which takes advantage of the fact that the bumps are distributed over the whole chip area and not just around the chip periphery.

A need has arisen for a low-cost leadframe structure, preferably pre-plated for reliable solderability. The leadframe and its method of fabrication should be flexible enough to be applied for different semiconductor product families and a wide spectrum of design and assembly variations, and should achieve improvements toward the goals of enhanced process yield and device reliability. Preferably, these innovations should be accomplished using the installed equipment base so that no investment in new manufacturing machines is needed.

SUMMARY OF THE INVENTION

One embodiment of the invention is a leadframe for use in the assembly of semiconductor chips. The leadframe includes a first plurality of segments, each segment of the first plurality having a narrow end portion in a first horizontal plane and a wide end portion in a second horizontal plane. The leadframe further includes a second plurality of segments, each segment of the second plurality

having a narrow center portion in the first horizontal plane, at least one wide center portion in the second horizontal plane, and narrow end portions in a third horizontal plane, which is located between the first and second planes. The wide segment portions may be covered by a layer of noble metal, preferably gold, or by a layer of solderable metal, preferably palladium. The narrow end portions of the first segment plurality and the narrow central portions of the second segment plurality may be covered by a layer of noble metal or a layer of solderable metal.

Another embodiment of the invention is a semiconductor device, which uses a leadframe as described above. The device further has an integrated circuit chip, which has on its active surface a first plurality of contact pads located in the peripheral chip portions, and a second plurality of contact pads centrally located; each of these pads has an interconnection element attached. The narrow end portions of the first plurality of leadframe segments are attached to the interconnection elements on the first plurality of chip contact pads, respectively. The narrow central portions of the second plurality of leadframe segments are attached to the interconnection elements on the second plurality of chip contact pads, respectively. The device further uses an encapsulation material, preferably a molding compound, which covers the chip and the leadframe segments, but leaves the wide portions of the first and second segment pluralities, located in the second horizontal plane, exposed. The chip interconnection elements are bumps made either of reflowable metal or alloy, preferably tin or a tin alloy, or of non-reflowable metal or alloy, preferably gold.

In another embodiment of the invention, the assembly of the semiconductor chip and the three-level leadframe are as described for the previous embodiment, but the encapsulation compound leaves the chip surface opposite to the active chip surface exposed. It is a technical advantage that a heat spreader or heat sink can thus be attached directly to the chip, creating a device with improved thermal characteristics.

In many embodiments of the invention, the first plurality of chip contact pads and the first plurality of leadframe segments serve as device signal inputs/outputs; the second plurality of chip contact pads and the second plurality of leadframe segments serve as device power and ground inputs/outputs. It is a technical advantage that this arrangement provides a low voltage drop of the power I/Os and the core regions of the chip, making these devices suitable for high power and high speed applications.

It is further a technical advantage of the invention that the second plurality of leadframe segments has the narrow end portions terminate in the third horizontal plane, remote from the second horizontal plane, in which the wide end portions of the first leadframe plurality are located. This feature allows a tighter segment pitch than would be feasible with an arrangement, in which all segment ends terminate in the same plane. The embodiments of the invention can thus not only accommodate low I/O counts (for example, 8 to about 100), but also intermediate I/O counts (for example, up to 200).

The technical advances represented by certain embodiments of the invention will become apparent from the following description of the preferred embodiments of the invention, when considered in conjunction with the

accompanying drawings and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic top view of an embodiment of the invention, illustrating a leadframe with two pluralities of segments for a flip-chip assembled device.

FIG. 2 is a schematic x-ray view of the leadframe in FIG. 1 after the forming step to create segment sections in three horizontal planes according to the invention.

FIG. 3 is a schematic bottom view of another embodiment of the invention, illustrating the assembly of a semiconductor chip onto a leadframe having segment sections in three horizontal planes.

FIG. 4 is a schematic x-ray side view of an embodiment of the invention, showing a semiconductor power device intended for low ground/power voltage drop.

FIG. 5 is a schematic x-ray side view of an embodiment of the invention, showing a semiconductor device with enhanced thermal performance.

FIG. 6 is a schematic top view of a leadframe in accordance with the invention.

FIG. 7 is a schematic x-ray side view of another embodiment of the invention.

FIG. 8 is a schematic x-ray side view of another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to U.S. Patent # 6,072,230, issued on June 6, 2000 (Carter et al., "Exposed Leadframe for Semiconductor Packages and Bend Forming Method of Fabrication"), and U.S. Patent Applications # 09/900,080, filed on July 6, 2001 (Abbott et al., "Preplating of Semiconductor Small Outline No-Lead Leadframes"), and # 10/346,899, filed on January 17, 2003 (Abbott, "Semiconductor Device with Double Nickel-Plated Leadframe").

FIG. 1 is a schematic and simplified top view of a leadframe, generally designated 100, for use in the assembly of semiconductor chips; FIG. 2 is a schematic x-ray view of leadframe 100 after the forming step. FIGs. 1 and 2 illustrate two pluralities of leadframe segments, held together by frame 101. Several segments of the first plurality are designated 110, and several segments of the second plurality are designated 120.

Each segment 110 of the first plurality has a narrow end portion 111 in a first horizontal plane 211 and a wide end portion 112 in a second horizontal plane 212. Each segment 120 of the second plurality has a narrow central portion 121 in the first horizontal plane 211, further at least one wide central portion 122 in the second horizontal plane 212, and narrow end portions 123 in a third horizontal plane 213. This third horizontal plane 213 is located between first plane 211 and second plane 212.

In the embodiments of the invention, the wide end portions 112 of the first segment plurality 110 have at least twice the width 111a of the narrow end portions 111. For practical fabrication reasons of the leadframes, the

narrow end portion width 111a has usually at least the dimension of the leadframe material thickness (typically between 100 and 300 μm).

As FIG. 2 shows, there have to be segment portions which are bent in order to provide continuous connection between the segment portions in the various horizontal planes. As examples, FIG. 2 depicts portions 114 if the first segment plurality and portions 124 and 125 of the second segment plurality. The degree of bending depends, among other parameters, on the leadframe material; see below.

In the preferred embodiments, the leadframe 100 is made of a base metal fully covered with a plated layer. As defined herein, the starting material of the leadframe is called the "base metal", indicating the type of metal. Consequently, the term "base metal" is not to be construed in an electrochemical sense (as in opposition to 'noble metal') or in a structural sense.

For many semiconductor devices, the base metal is typically copper or copper alloys. Other choices comprise, but are not limited to, brass, aluminum, iron-nickel alloys ("Alloy 42"), and invar.

The base metal originates with a metal sheet in the preferred thickness range from 100 to 300 μm; thinner sheets are possible. The ductility in this thickness range provides the 5 to 15 % elongation that facilitates the segment bending and forming operation. The leadframe is stamped or etched from the starting metal sheet.

After the stamping or etching process, the leadframe is plated. In order to illustrate an example of the structure of the plated layers, a cross section of a segment of the first plurality is administered along line

A-A' in FIG. 1 and shown in FIG. 3. The schematic cross section of the leadframe segment in FIG. 3 shows the base metal 301 and the first plated layer 302 on both surfaces of the base metal sheet 301. For many embodiments, layer 302 comprises nickel having a thickness between 0.2 and 1.0 μm, preferably 0.5 ± 25 μm. Nickel is the preferred metal because, positioned under the tin-based solder of contemporary devices, it reduces the propensity for tin whiskers. Frequently, this nickel is rough and non-reflective; it is sometimes referred to as "TN nickel". The roughness of the nickel surface promotes adhesion between the nickel-plated leadframe and the molding compounds used for encapsulating semiconductor devices.

The plated layer is ductile for the leadframe segment bending and forming process. However, due to its rough surface, the rough nickel layer is visually very dull and non-reflective. Consequently, it may complicate the vision systems of automated semiconductor assembly steps requiring image recognition or alignments so that sometimes a plated nickel with smooth surface is preferred. However, this smooth nickel, commonly sulfamate nickel, does not adhere well to molding compounds. Therefore, sulfamate nickel may either be deposited only on surfaces where visual image recognition requires it for facilitating assembly steps (see cross section along line A-A' in FIG. 4, layer 401), or alternatively the sulfamate nickel may be covered with an additional adherent thin layer of palladium, gold, or alloys thereof, which promote adhesion to molding compounds. The sulfamate nickel layer is ductile for the leadframe bending and forming process. Further, both the rough and the smooth nickel layers are

wettable in the soldering process, so that tin or solder alloys can be used successfully.

It is preferred that leadframe 100 comprises spots of additional plated layers, which promote the assembly steps of flip-chip attachment and external device attachment. For the flip-chip assembly step, two scenarios have to be considered, see FIG. 5. In the first scenario for embodiments with reflowable interconnection elements on the chip I/O pads, such as a tin alloy, adherent layer 501 is made of metals, which are solderable. In addition, metal surfaces intended for external solder attachment have adherent layer 502 made of metals, which are solderable. Examples for layers 501 and 502 include palladium, gold, platinum, silver, rhodium, or nickel as single metals or as alloys. These metals also have an affinity to molding compounds. The thickness of layers 501 and 502 is preferably in the range from 20 to 60 nm, but could, for cost reduction reasons, possibly be reduced to 10 to 30 nm.

Alternatively, layer 502 may be plated as a solder layer comprising, for example, tin or a tin alloy. While the semiconductor technology offers the option to deposit this solder layer after completion of the encapsulation step, it is preferred to deposit layer 502 before encapsulation in order to avoid the risk of delamination. This option is often referred to as pre-plating.

In the second scenario for embodiments with chip interconnection elements made of non-reflowable metals, such as gold, adherent layer 501 is made of non-oxidizing (noble) metals, which provide reliable electrical contact to the non-reflowable interconnection element. For this case, examples for layer 501 include gold, palladium,

platinum, silver, or alloy thereof, preferably in the thickness range from 10 to 30 nm.

In the segment forming process step after completion of the layer depositions, the segments obtain a three-plane configuration as exemplified in FIG. 2. By way of explanation, an outside force, applied along the length of the segment, can stretch the segment in the direction of the length, while the dimension of the width is only slightly reduced, so that the new shape appears elongated. For elongations small compared to the length, and up to a limit, called the elastic limit given by the material characteristics, the amount of elongation is linearly proportional to the force (beyond that elastic limit, the segment would suffer irreversible changes and damage to its inner strength and could eventually break).

When a distance between planes on the order of about 400 to 500 µm has to be bridged, this challenge can usually be met while staying within the limits of material characteristics, if the distance is bridged by the segment at an inclination angle of 30° or less. For instance, with copper as basic element of the sheet material for the leadframes (thickness range 100 to 300 µm), appropriate alloys combined with suitable thermal treatment can be selected so that leadframes can be designed with straight segments capable of sustaining forced stretches to cover that distance at "shallow" angles (30° or less). If necessary, a multi-step configuration at angles of 40° or less can be adopted for covering that distance. As a side benefit, this configuration enhances mold locking of plastic to the leadframe in transfer molded plastic packages.

In some devices, the direct distance of 400 to 500 µm between the planes may have to be bridged at angles steeper then 30°, for instance 45°; this need may happen in order to shrink the outline of a package (that is the area it consumes when mounted on a printed wiring board) as much as possible, or to accommodate an extra large chip pad in a given package. A copper segment elongation of more than 8 % would be required, which is beyond the elastic limit of copper leadframe materials.

A twofold approach provides solutions for this need: Linearizing a designed-in bending, and stretching through forming. The contribution of linearizing can be obtained when a topologically long body is first designed so that it contains curves, bendings, meanderings or similar non-linearities. By applying force, at least part of the non-linearities is stretched or straightened so that afterwards the body is elongated. The contribution of stretching is similar to the elongation in the direction of the segment length discussed above. This stretching, therefore, will remain safely below the elastic limit of the leadframe material.

In the example of a leadframe with the segments in three planes, FIG. 1 configures the segments 110 of the first plurality so that each segment has a narrow end portion 111 and a wide end portion 112; for many device applications, it is practical to configure the wide end portion at least twice as wide as the narrow end portion. The segments 120 of the second plurality have narrow central portions 121 and end portions 123 combined with wide central portions 122. A leadframe with these features is depicted in FIG. 6 for use in the assembly of a chip 601 to create a semiconductor device generally designated 600.

Chip 601 has on its active surface 602 an integrated circuit with a first plurality of contact pads 603 generally located on the peripheral chip portions, and a second plurality of contact pads 604 generally located on the central chip portions. Each of these contact pads 603 and 604 has an interconnection element attached; the elements 703 and 704 are indicated in the schematic x-ray FIGs. 7 and 8. As stated above, the interconnection elements may be made of a reflowable alloy such as tin alloy, or a non-reflowable alloy such as gold alloy. In many devices, the contact pads of the first plurality serve as device signal inputs/outputs, and the contact pads of the second plurality serve as power and ground inputs/outputs.

Referring to FIG. 6, the narrow end portions 111 of the first segment plurality 110 are attached to the interconnection elements on the peripheral chip contact pads 603. The narrow central portions 121 of the second segment plurality 120 are attached to the interconnection elements on the centrally located chip contact pads 604. The method of attachment depends on the material of the interconnection elements. For elements made of reflowable material, the attachment step involves a soldering process, for elements made of non-reflowable material, the attachment step involves a thermo-compression process.

The schematic x-ray FIGs. 7 and 8 display the position of chip 601 relative to the three segment planes 211, 212, and 213 of leadframe 100 after completing the assembly steps. FIGs. 7 and 8 further illustrate the completion of the device by protecting chip and leadframe segments with encapsulation material, and then performing the trimming step of the frame. In FIG. 7, a device,

generally designated 700, is formed by encapsulating chip 601 from all sides together with most of the leadframe segments, leaving exposed only those external-facing surfaces of the wide segment portions of the first and second segment pluralities, which are located in the second horizontal plane 212. In FIG. 7, the encapsulation material is designated 730, and the exposed segment surfaces are marked 712a and 722a. A preferred choice for the encapsulation material 730 is an epoxy-based molding compound with silicate and alumina fillers, which permits the usage of the well-controlled transfer molding method.

FIG. 8 shows an embodiment, in which the encapsulation material 830 also leaves the passive surface 603 of chip 601 exposed. The embodiment of FIG. 8 is favored by devices with a need for enhanced thermal characteristics. A heatsink or other good thermal conductor can be attached to chip surface 603, enabling improved heat removal and chip cooling.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the material of the semiconductor chip may comprise silicon, silicon germanium, gallium arsenide, or any other semiconductor or compound material used in IC manufacturing.

As another example, the process step of stamping the leadframes from a sheet of base metal may be followed by a process step of selective etching, especially of the exposed base metal surfaces in order to create large-area

contoured surfaces for improved adhesion to molding compounds.

It is therefore intended that the appended claims encompass any such modifications or embodiments.